

CSE 460

VLSI LAB

ASSIGNMENT 06

**Submitted by**

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CSE-460 Fall-2022

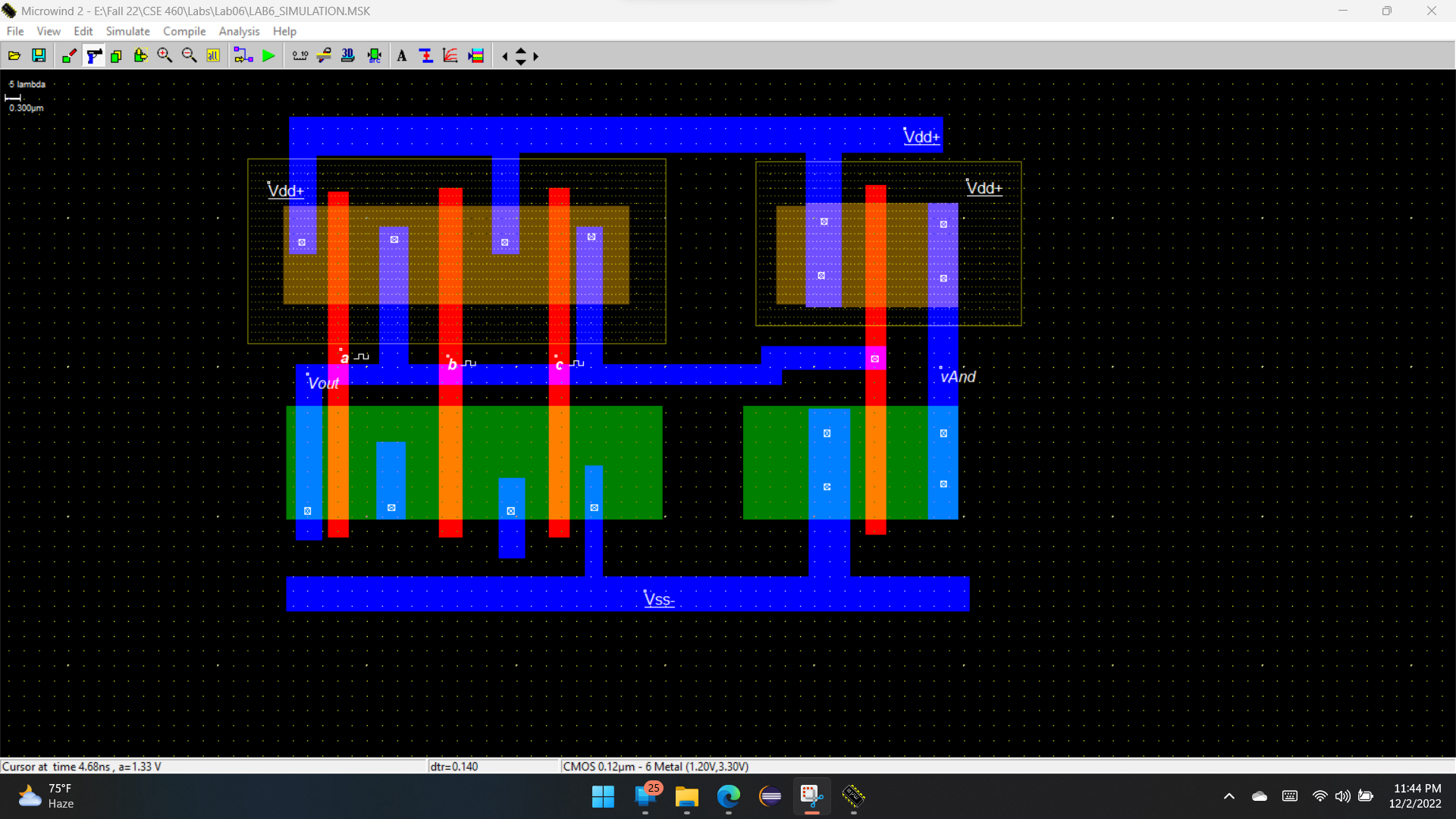
Submission Date: 2nd December 2022

**Lab Assignment 06**

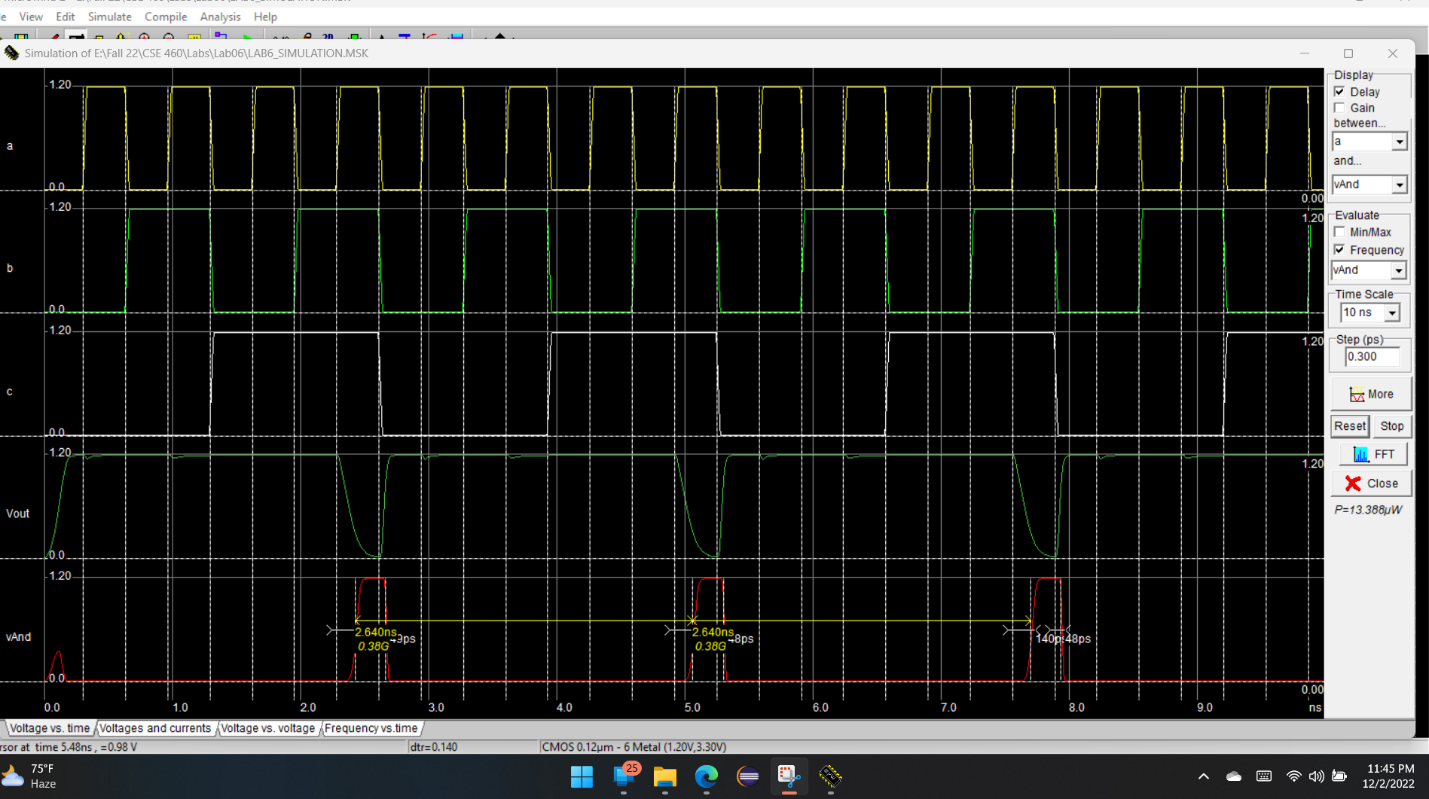
**Problem statement**

Draw the layout of AND3 and verify it with the timing diagram. Take ss of the layout and the timing diagram, and briefly explain whether the timing diagram matches with the AND3 truth table..

**Simulation of cMOS AND layout**



**Timing Diagram**



**Explanation of how the timing diagram manifests the Truth Table**

